

Extensions to the IEEE 1149.1 boundary-scan standard

DESPITE THE SUCCESS OF THE IEEE 1149.1 BOUNDARY-SCAN STANDARD, ACCEPTANCE OF THE 1149.4 MIXED-SIGNAL EXTENSION HAS BEEN SLOW. THE INDUSTRY BADLY NEEDS THAT EXTENSION AND OTHERS, HOWEVER, AND SEVERAL COMPANIES ARE HARD AT WORK TO PUT THEM ON THE FAST TRACK.

The IEEE 1149.1 boundary-scan standard was developed almost 15 years ago to resolve the problems associated with limited physical access for probing test points on pc boards and to verify that device pins have been soldered correctly and are free of solder shorts and open circuits. However, the test industry now faces new problems that nobody envisioned when the standard was developed back in 1990, and a number of working groups have engaged in a sustained effort to develop new standards that build on the success and acceptance of IEEE 1149.1.

More recent standards that extend 1149.1 are 1149.4, the mixed-signal test-bus standard for testing analog pins; 1149.6 for testing the interconnections between ac-coupled differential nets; and IEEE 1532 for the in-system configuration of programmable devices.

The 1149.4 standard specifies that every signal pin must be associated with a boundary module, which in the case of the digital pins is referred to as a DBM (digital-boundary module). DBMs are identical to the boundary-scan cells defined in 1149.1. Mixed-signal pins are associated with ABMs (analog-boundary modules). Each ABM consists of a switching network that allows the mixed-signal pin to be disconnected from the core circuitry in the CD (core-disconnect) state and allows it to connect to the internal bus or the internal dc reference voltages. Alternatively, if the PROBE instruction is selected, the network leaves all pins in functional mode and allows the pins' signal to be measured via the internal analog bus (Reference 1).

Figure 1 shows the construction of a simple mixed-signal device that consists of sev-

eral DBMs and ABMs, which are selected through the TAP (test-access port), as defined in 1149.1, and an ATAP (analog test-access port), which supports 1149.4's analog stimulus-and-response capabilities. This arrangement requires two extra AT (analog-test) pins: AT₁ for providing an external test stimulus and AT₂ for routing signals connected to the associated ABMs to external measurement instrumentation.

The external analog-test bus, which connects to AT₁ and AT₂, accesses an internal bus under the control of the TBIC (test-bus interface circuit). The TBIC allows the internal test-bus

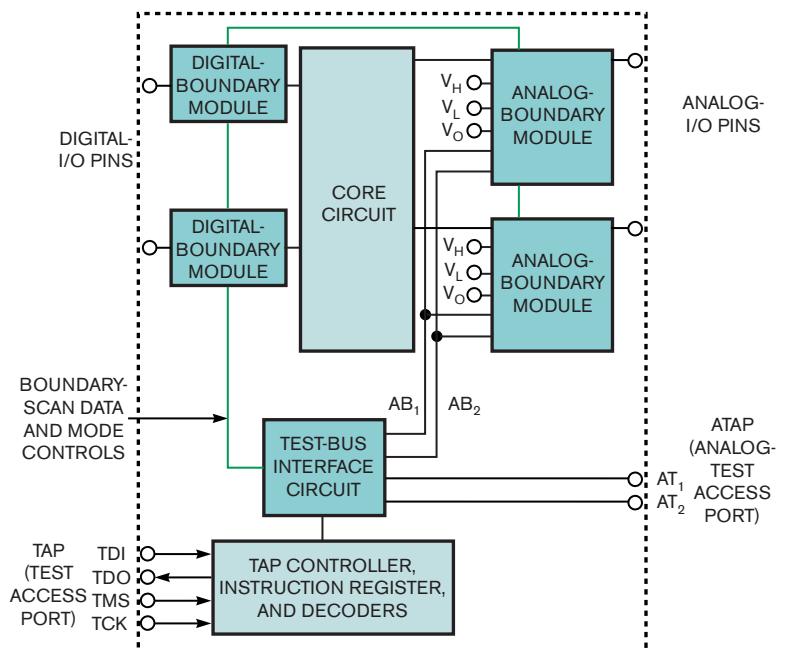


Figure 1 In this simple chip, boundary-scan features surround the core.

lines to connect to either or both ATAP pins, isolates the internal test bus when it is not in use to eliminate unwanted noise interference, or connects the bus to one of two dc voltages (V_H and V_L), which act as logic values for performing standard dc interconnect testing (Figure 2).

CONTROLLING ABMs

A 4-bit register controls each ABM. The register is part of the boundary-scan data register and can capture digital-test results that represent either logic values or digitized analog responses. As can the DBMs, the individual control registers can load and unload through the 1149.1 TAP.

The four bits are C, D, B_1 , and B_2 (control, data, $ABUS_1$, and $ABUS_2$). The C bit acts as an enable pin, and the D bit provides the pin's logic values, V_H and V_L . When the C and D bits are both zero, the pin is disconnected from the core through the CD switch. B_1 and B_2 control the switches that connect the signal pin respectively to the AB_1 and AB_2 test-bus lines.

The 1149.4 standard requires support for one more instruction than those for which 1149.1 mandates support. This instruction is PROBE, whose primary purpose is to allow real-time access to signal pins without affecting the UUT's (unit under test's) normal operating mode. In effect, the PROBE instruction is similar to SAMPLE/PRELOAD and allows virtual probing of selected IC pins without impacting their normal function.

At the board level, a single boundary-scan path can link any combination of 1149.1- and 1149.4-compliant devices, with the TDO (test-data-out) pin of one device connected to the TDI (test-data-in) pin of the next. The TCK (test-clock) and TMS (test-mode-select) pins connect in parallel as defined in 1149.1. Similarly, the AT_1 and AT_2 pins connect in parallel to the 1149.4-compliant devices (Figure 3).

DEVELOPMENTS

Although 1149.4 was approved in June 1999, the industry has been slow in adopting it. More important, IC vendors have been slow to produce devices that would enable board designers to use and experiment with the technology. To stimulate interest in implementing 1149.4, National Semiconductor (Reference 2), an innovator in analog semiconductors, and LogicVision, a provider of embedded-test intellectual property for ICs and systems, collaborated on developing the first general-purpose IEEE 1149.4-compliant IC, the STA400 (Figure 4).

The STA400 is mainly an evaluation chip whose core functions primarily as a simple analog multiplexer comprising 11 ABMs that can connect to circuit nodes to enable injection of a test stimulus or monitoring of discrete dc voltages and ac signals. You can use the chip to determine values of discrete passive components by injecting currents at different signal nodes, measuring the resultant voltage at each node, and calculating the value of the selected components.

JTAG Technologies has developed an IEEE 1149.4 evaluation kit that uses STA400s to let users select circuit nodes and perform resistance, capacitance, voltage, ac-signal, and characteristic-impedance measurements on an evaluation board

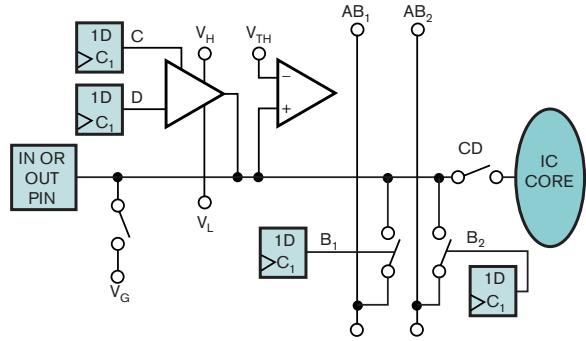


Figure 2 This analog-boundary module resides on an IEEE 1149.4 IC and allows you to connect an I/O pin to the IC's core or to either of two analog buses.

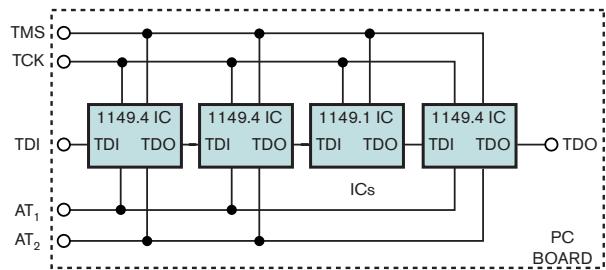
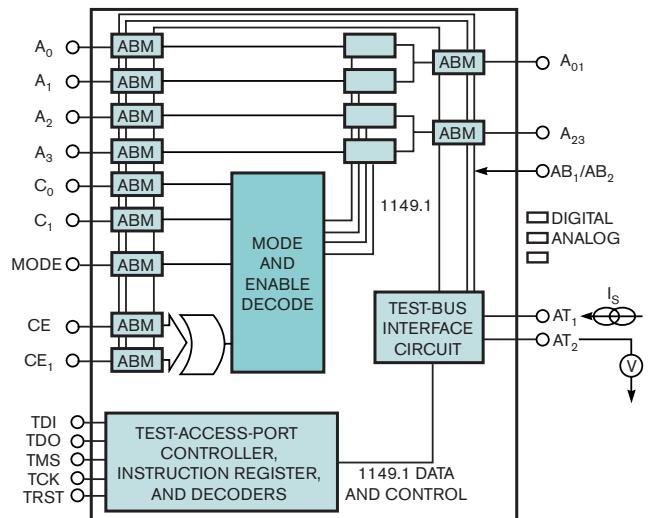


Figure 3 On the pc board, the analog-test buses, AT_1 and AT_2 , connect to multiple ICs.



NOTE:
ABM=ANALOG-BOUNDARY MODULE.

Figure 4 The STA400 evaluation chip allows you to experiment with 1149.4-based test concepts.

using a graphical user interface. In another application of this system, you can perform analog measurements on target boards by using the test resources (stimulus and measurement instrumentation) of the JTAG-1149.4 Explorer package (references 3 and 4).

AC-COUPLED DIFFERENTIAL NETS

IEEE 1149.6 was developed to address the requirements of boundary-scan testing of ac-coupled differential nets. Coupling capacitors on high-speed digital interconnects block dc signals and prevent receivers from detecting them. Using an R-C network causes signals to decay over time, typically requiring at least 2.5 TCK cycles between driving a net and capturing a signal.

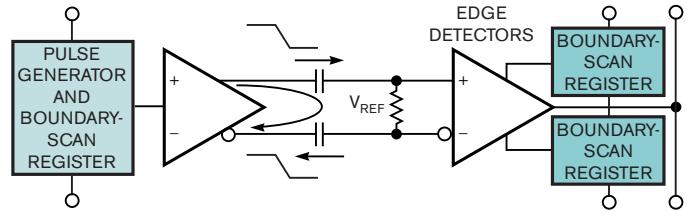
The basic implementation of 1149.6 requires adding to the signal-path driver a generator that can transmit a single pulse or a train of pulses depending on whether the EXTEST_PULSE or EXTEST_TRAIN instruction is loaded into the 1149.1 instruction register. A test receiver located behind the receiving-device pins detects a steady-state level or captures edge transitions (Figure 5). The test receiver must be able to support both of these new instructions as well as the traditional static 1149.1 EXTEST. When the IEEE 1149.1 EXTEST instruction is active, the receiver must revert to level sensing, whereas, when one of the new 1149.6 instructions is active, the receiver must capture edge transitions.

When the interconnection between the driver and the receiver is dc-coupled, the receiver must detect levels by referencing the input signal to a dc-bias voltage that the ac-mode-control signal selects (Figure 6). When the interconnection between the driver and the receiver is ac-coupled, the transitions at the receiver's input pins are detected by comparing the input signal with a delayed version of itself. In this self-referencing technique, the lowpass filter provides the signal delay. In Figure 7, the upper comparator detects rising edges, and the lower comparator detects falling edges. These comparator outputs respectively set and clear the receiver flip-flop, reproducing the original waveform at output C regardless of whether the input signal, A, is dc- or ac-coupled.

With the proliferation of multigigabit-per-second serial-data-communication protocols, a significant number of devices will likely implement 1149.6. In fact, several 1149.6-enabled devices are already available (Reference 5), and tools are in development to enable 1149.6 insertion and verification. Vendors are also upgrading board-test software to enable testing of 1149.6 components and their interconnections to other onboard boundary-scan-compliant devices.

IN-SYSTEM PLD CONFIGURATION

For many years, the test industry has been asking for some level of standardization for ISC (in-system con-



NOTES:
PULSE GENERATOR AND BOUNDARY-SCAN REGISTER SUPPORT
IEEE 1149.1 INTERCONNECT AND OFFER EDGE GENERATION/DETECTION
FOR AC-COUPLED TESTS.

Figure 5 IEEE 1149.6 allows you to use boundary-scan technology to test such differential analog structures as drivers and receivers for ultrahigh-speed serial buses.

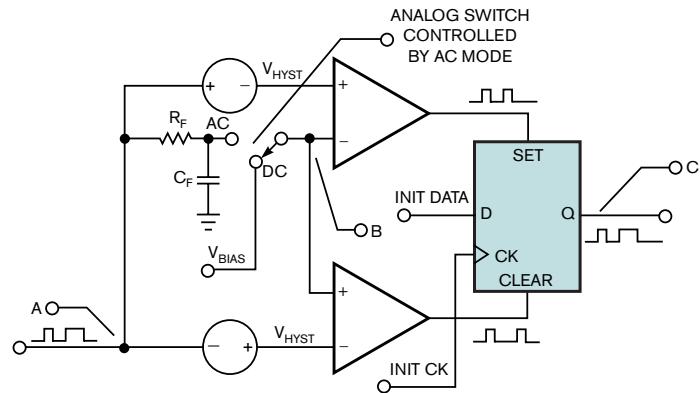


Figure 6 In this circuit, when the interconnection between the driver and the receiver is dc-coupled, the receiver must detect levels by referencing its input to a dc-bias voltage that the ac-mode-control signal selects.

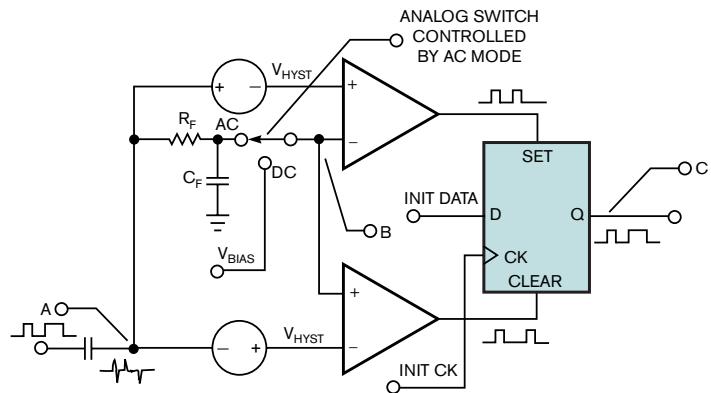


Figure 7 When the interconnection between the driver and the receiver is ac-coupled, the transitions at the receiver's input pins are detected by comparing the input signal with a delayed version of itself.

figuration) of programmable devices. In the past, suppliers of programmable ICs have used programming algorithms that differed not only among vendors, but also among device families from the same vendor.

The silicon portion of IEEE 1532 establishes common device behavior during programming via the IEEE 1149.1 state machine. The software portion of the standard defines a modified BSDL (boundary-scan-description-language) file, which extends to cover the new ISC instructions. Additionally, a new

ISC data-file format contains all of the device and pattern-specific programming information.

By delivering faster programming and facilitating more efficient use of expensive testers, the ISC features of 1532-compliant ICs provide significant savings to equipment manufacturers.

Users will now be able to program chains of complex PLDs from multiple vendors using the same third-party programming tools and controllers.

Users will no longer need vendor-specific programming knowledge and will be able to concurrently program multiple PLDs from different IC vendors. Devices that are programmed concurrently instead of sequentially will simultaneously enter and leave programming wait states, minimizing configuration

time, significantly reducing overall programming time, and allowing design needs, rather than programming-equipment availability, to govern programmable-device selection. **EDN**

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- 4 IEEE 1149.4 Mixed-Signal Test-Bus Working Group, <http://grouper.ieee.org/groups/1149/4/index.html>.
- 5 National Semiconductor, SCAN90CP02 Crosspoint Switch, www.national.com/appinfo/scan/cp02.html.

AUTHOR'S BIOGRAPHY

Peter Collins has worked in the test industry for 25 years and now works for JTAG Technologies in technical marketing. Before joining JTAG, he worked for eight years with Motorola in Swindon, UK, where he developed test approaches for GSM base-station pc boards. He was also jointly responsible for defining Motorola's corporate strategy for implementing 1149.1 in the factory and in the field. You can reach him at petec@jtag.co.uk.

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